

# Thrust 3: Electrical Characterization Overview

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G A T O R  
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UNIVERSITY OF  
FLORIDA

# Outline

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- Overview-Electrical Characterization
- Device Modification/Defect Generation
- Characterization
- Related Results and Preliminary Models

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# Overview

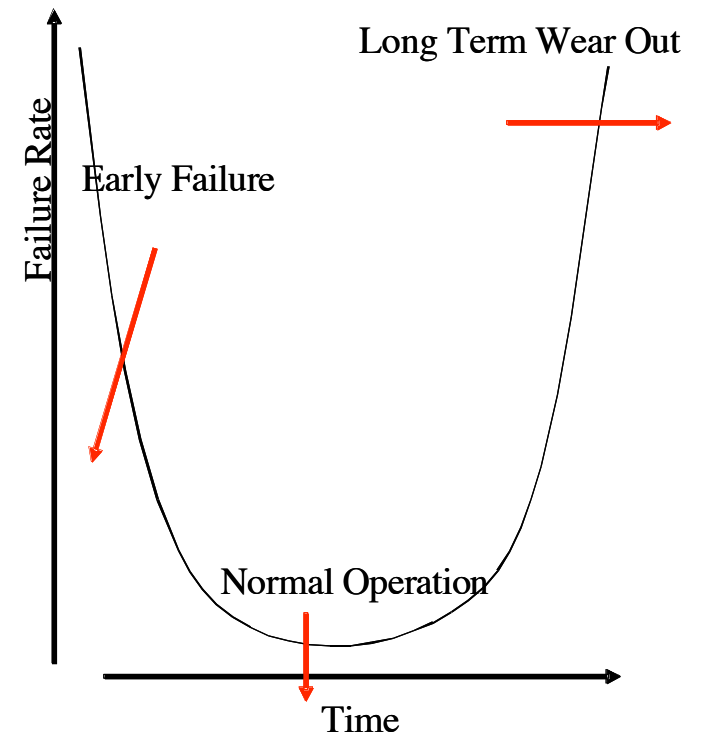
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- Tightly integrated approach
  - Test structure fabrication
  - Materials characterization
  - Electro(thermo)(opto)(mechano) characterization
    - Device modification/Defect generation
      - Electrical (DC and RF), mechanical, thermal, optical stresses
    - Characterization
  - Modeling
  - Statistics



# Overview

- Goal
  - Employ multiple characterization vectors
  - Gain insight into physical degradation mechanisms
  - Feedback into predictive models
  - Compare predictions with characterization results
    - Collect sufficient statistics for confidence
    - Design high performance and high reliability compound semiconductor electronics



# Outline

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- Overview-Electrical Characterization
- **Device Modification/Defect Generation**
- Characterization
- Related Results and Preliminary Models

# Device Modification/Defect Generation

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- Electrical stress (DC and RF)
- Mechanical stress
- Thermal stress
- Optical stress

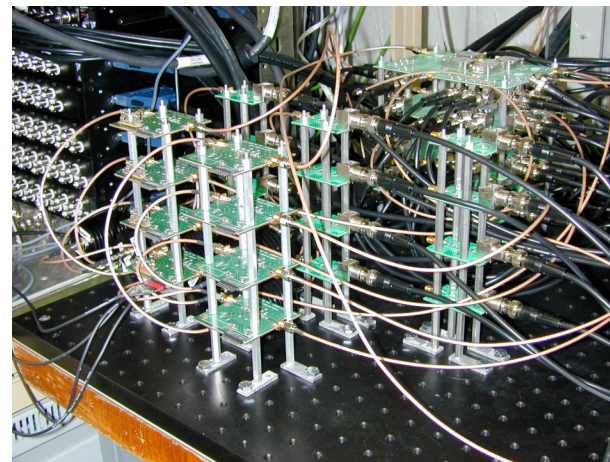
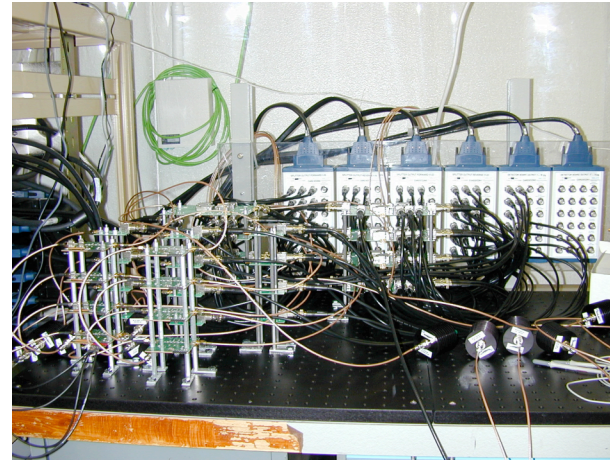
# Device Modification/Defect Generation

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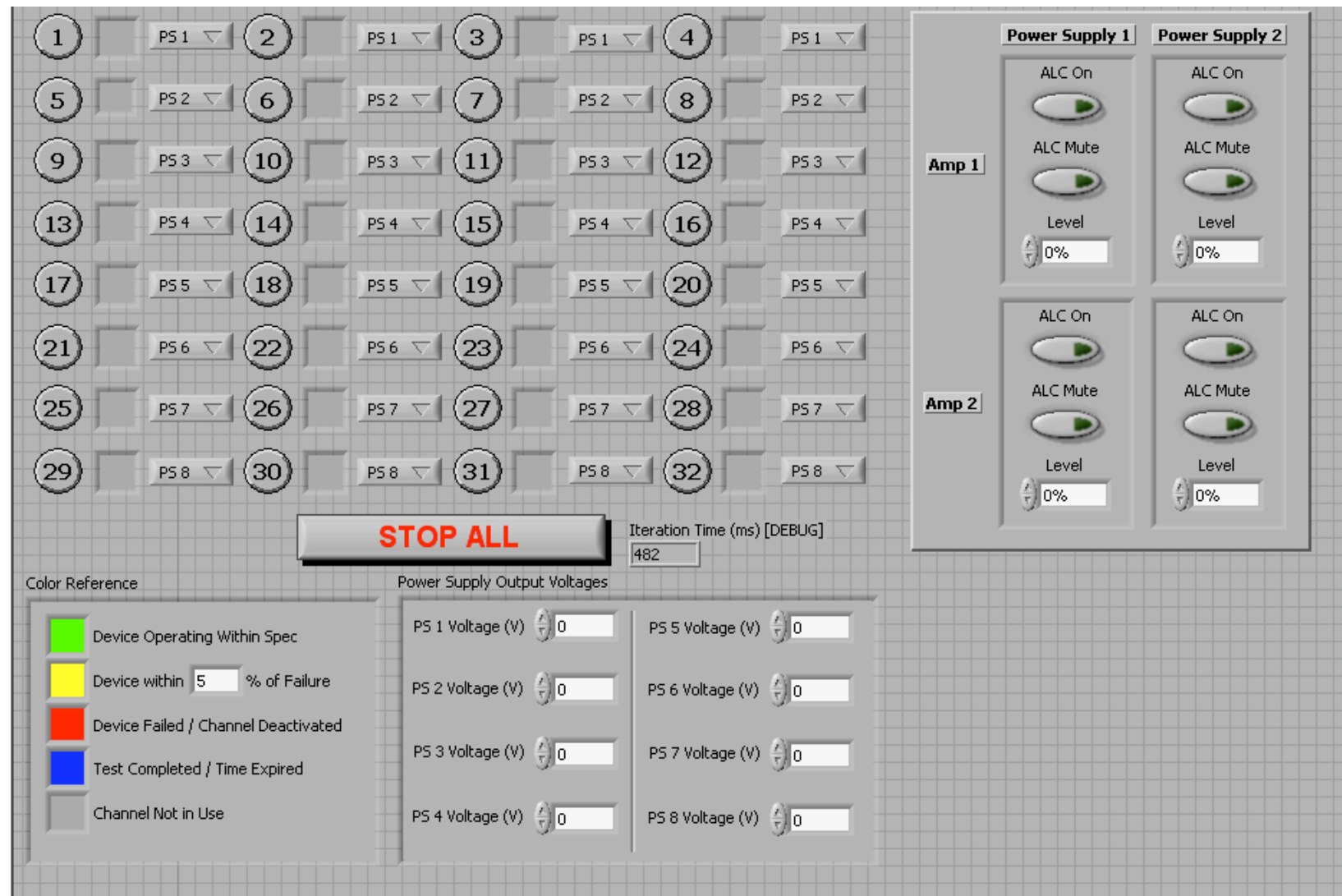
- Electrical stress (DC and RF)
- Mechanical stress
- Thermal stress
- Optical stress

# Burn-In Test System


- Supply voltage and current stressed devices to other MURI members for characterization- similar to Accel-rf but modular.
  - Provide enough samples to produce realistic statistics.
  - Currently 8 channels- expandable to 32, operational range 25-150°C, 0-60V, 5W.
  - Will integrate IR camera and illumination source.



# Master System Monitor



# Single Device Monitor

On / Off 

Data File  
C:\Testrun.xls

Test Mode **Constant Drain/Collector**

Autosave Every 1 Hours

Wafer Name / Batch Descriptor  
eb3242

Part Prefix Part Number  
NT 0001

Performed By  
Torben F.


Comments

Maximum Experiment Duration  
1 Hours

Time Elapsed  
0:00:00:00

Stress Mode Present Stress Level  
Normal 100 %

Failure Level 0 %  
Samples Past Fail 5

Attenuator connected? 

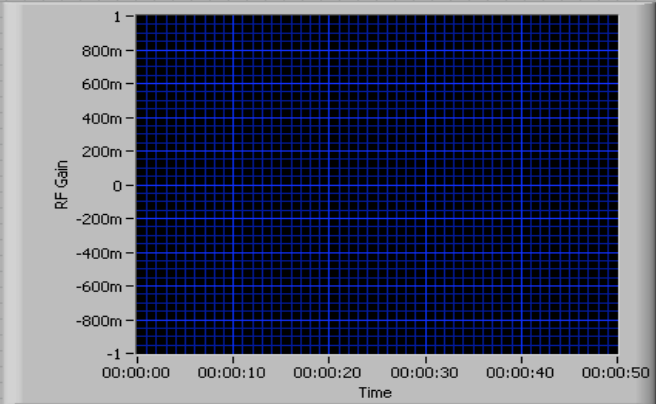
Gate/Base Monitor Resistor 0 ohms  
Gate/Base Control Voltage 0 V  
Gate/Base Control Current Inf A  
Gate/Base Monitor Voltage 0 V  
Gate/Base Monitor Current Inf A  
Gate/Base Voltage (Vbe) 0 V  
Drain/Collector Supply Voltage 0 V  
Drain/Collector Voltage (Vce) -51.5804m V  
Drain/Collector Monitor Resistor 100m ohms  
Drain/Collector Ext Resistance 0 ohms  
Drain/Collector Control Current 0 A  
Drain/Collector Monitor Current 515.804m A  
Drain/Collector Monitor Voltage 51.5804m V  
Control Voltage Start -4 V  
Splitter Forward Power NaN dBm  
Splitter Reverse Power NaN dBm  
Detector Output Power NaN dBm

Sample Time Intervals

| Initial Sample Rate (t1) | 1     | sec |     |
|--------------------------|-------|-----|-----|
| After 1                  | Hours | 5   | sec |
| 1                        | Hours | 5   | sec |
| 1                        | Hours | 5   | sec |
| 1                        | Hours | 5   | sec |

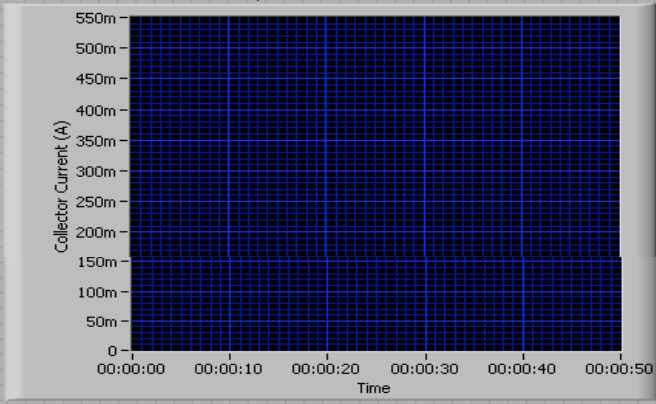
Clear/Reset Settings Save Data Now Plot Buffer Size 200

RF Gain vs. Time



RF Gain Max 0 A RF Gain Median NaN A

Drain / Collector Current vs. Time



Drain/Collector Max (I) 0 A Drain/Collector Median (I) NaN A



# Device Modification/Defect Generation

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- Electrical stress (DC and RF)
- Mechanical stress
- Thermal stress
- Optical stress



# Sources of Mechanical Stress

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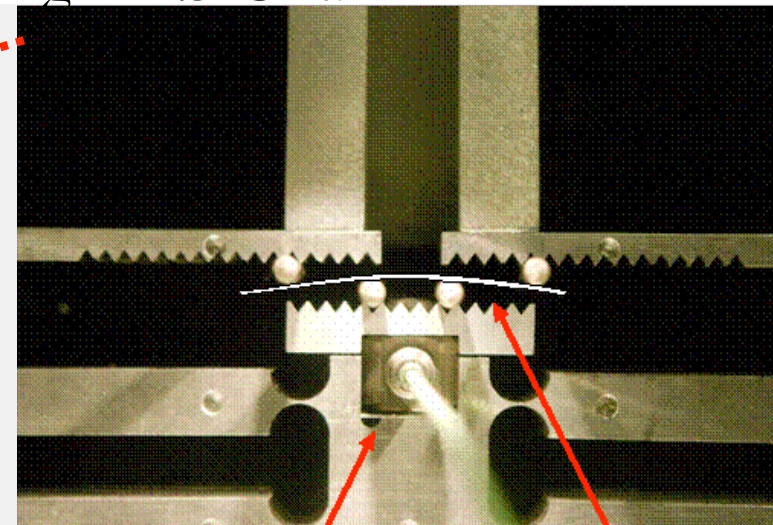
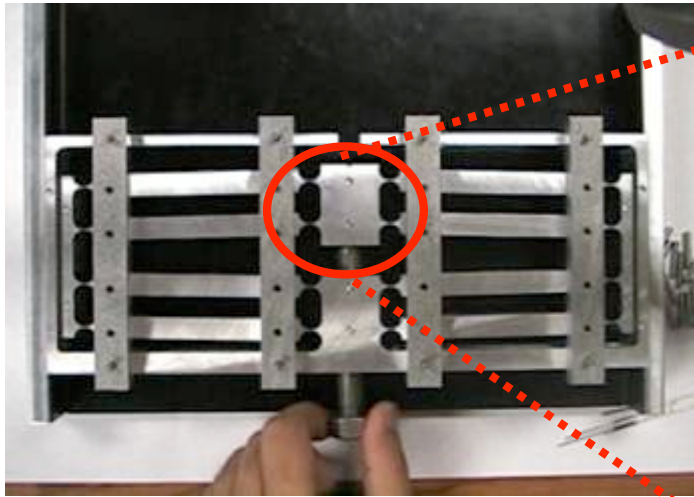
- Fabrication process-induced mechanical stress
  - Lattice mismatch
  - CVD thin film residual stress
  - Dopant-incorporation
- Bias-induced stress via inverse piezoelectric effect
- Package/Encapsulation/Operational stress
  - Thermal coefficient of expansion mismatch
  - Intermetallic growth

>> Varying process stress may change device <<

➤ Controlled applied mechanical stress

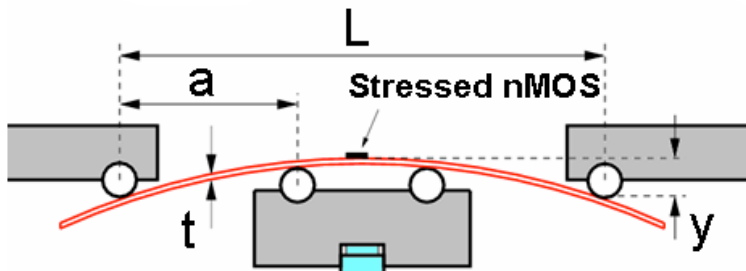
# Externally Applied Mechanical Stress

- Flexure based four point bending jig
  - Highest to date wafer bending  $\sim 1.5$  GPa



Pressure  
sensor

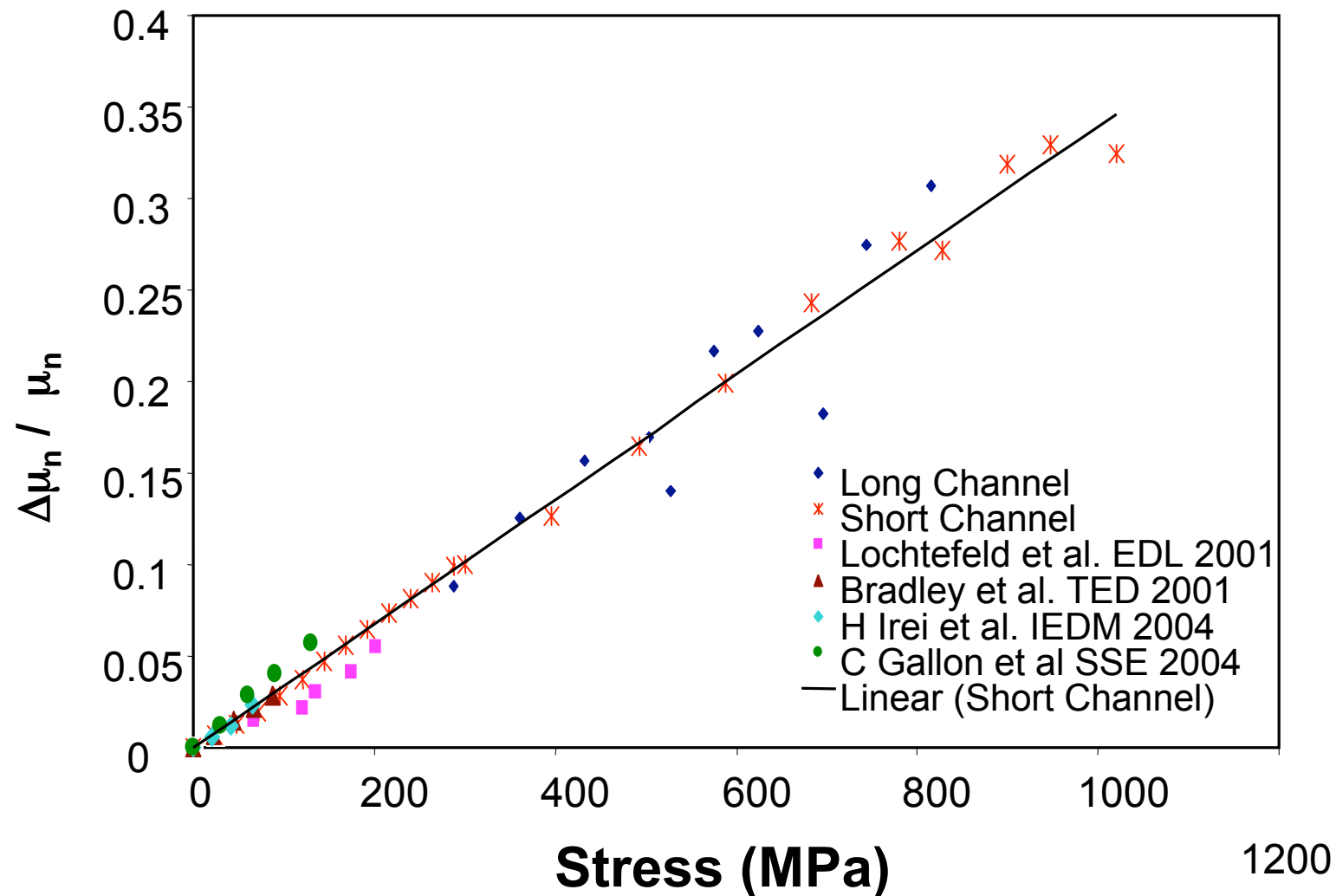
Wafer



$$\sigma = \frac{Eyt}{2a \left( \frac{L}{2} - \frac{2a}{3} \right)}$$

Ref: S. Suthram et al., "Piezoresistance Coefficients of (100) Silicon nMOSFETs Measured at Low and High ( $\sim 1.5$  GPa) Channel Stress", IEEE Electron. Dev. Lett., Vol. 28, pp. 58 – 61, January 2007

# Electron Mobility Enhancement in Si nMOSFET



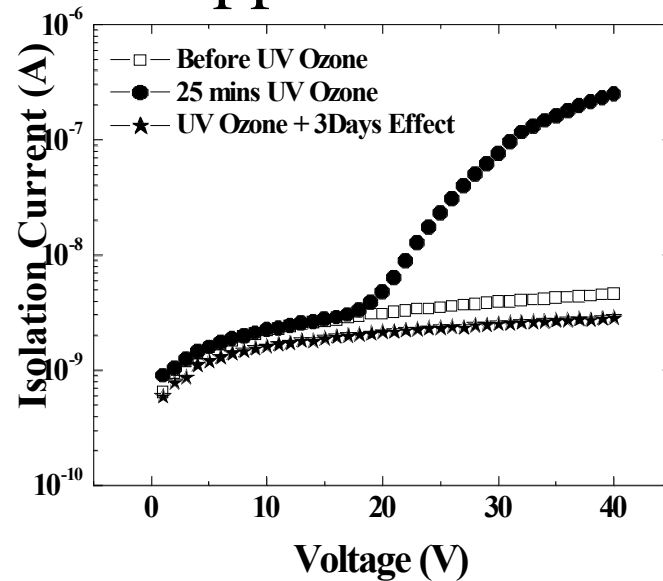
# Device Modification/Defect Generation

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- Electrical stress (DC and RF)
- Mechanical stress
- Thermal stress
  - Active heating from electrical stress
  - Calibration via passive heating
- Optical stress
  - UV stress of materials

# UV Stress

- Excitation of trapped carriers in material layers



- Initial dark isolation current baseline
- UV stress-induced increase in isolation current
- Recovery time for post dark isolation current
  - Go/No-go digital test
  - Integrate with other stressors to investigate defect generation/relaxation and capture/emission

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- Overview-Electrical Characterization
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- Related Results and Preliminary Models

# Characterization

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- On-state and off-state currents
- Stress and recovery transients
- Noise characterization
- IR and uRaman

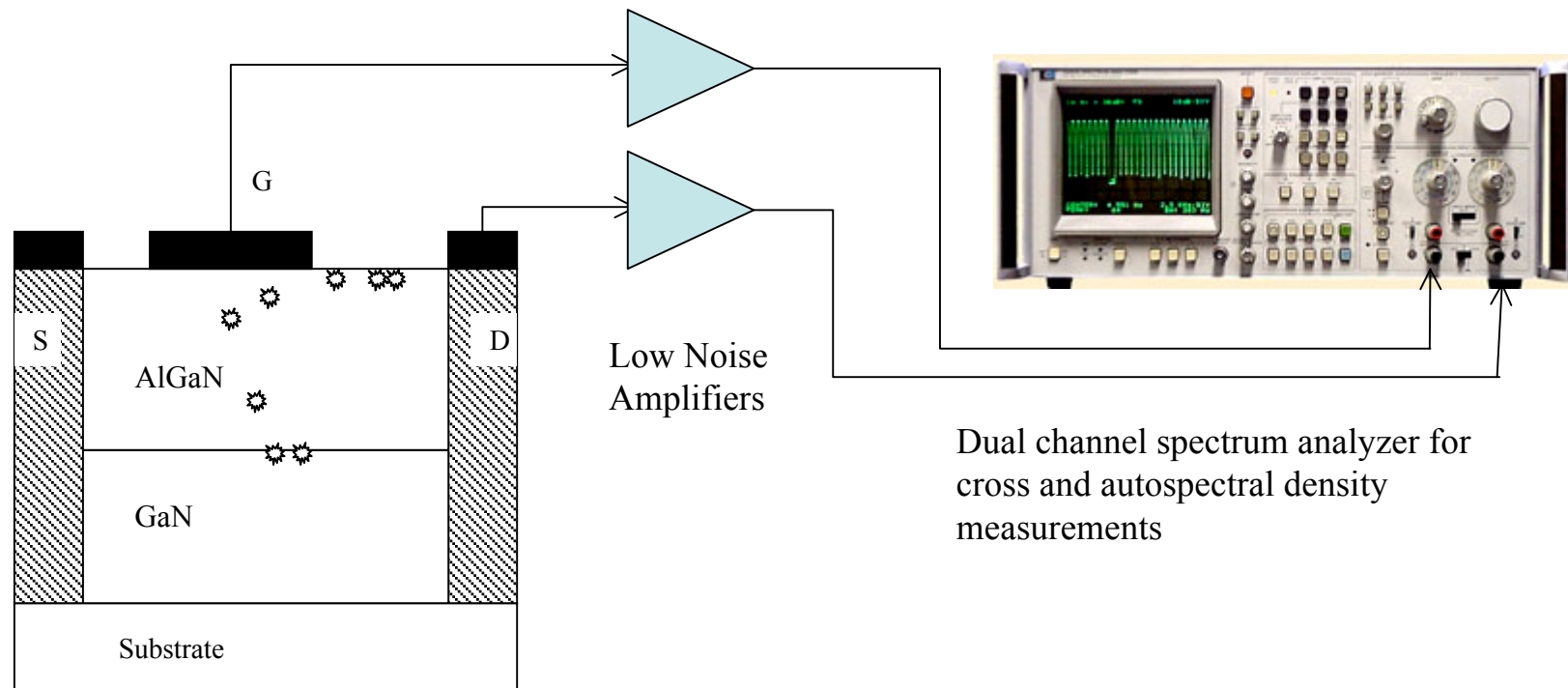
# Noise Characterization

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- Noise signatures
  - Only due to defects that interact directly with charge carriers
- Technique
  - Employs standard devices
  - Measures drain and gate current PSD
    - Frequency dependent component at low frequencies
    - Frequency independent



# Experimental Noise Setup for an AlGaN/GaN HEMT



- ⚙ Possible locations of hot electron or reverse piezo electric induced traps generating noise

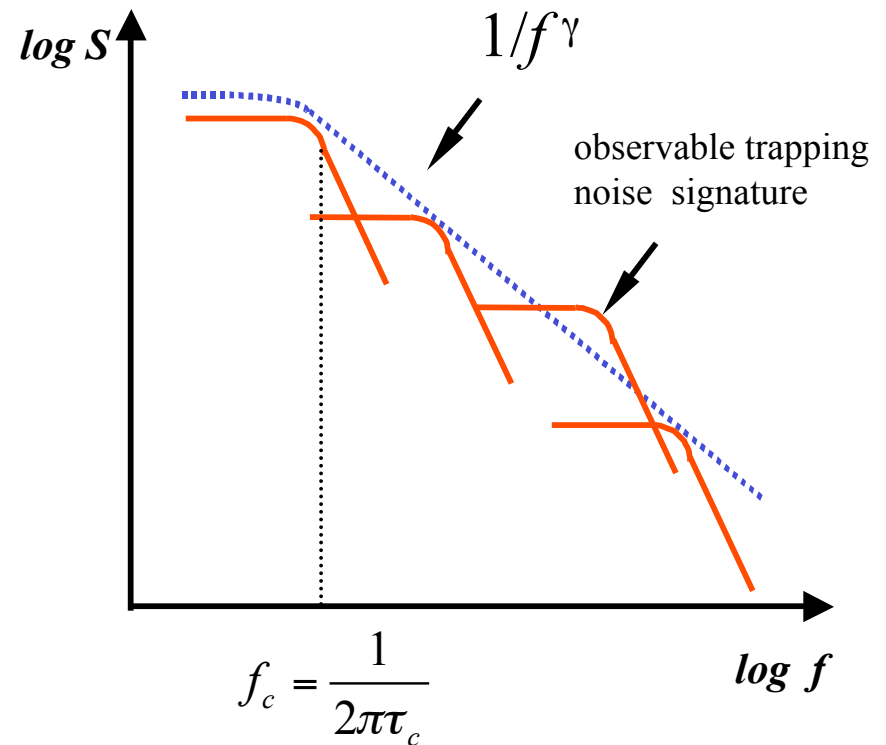
# Defect Noise Spectroscopy

## Advantages of Noise Spectroscopy

- Only defects that actually affect charge transport are probed in actual devices and under realistic bias conditions.
- Microscopic noise signatures provide early warning of macroscopic breakdown.

## Data Extraction

- Measured low frequency noise spectra typically consist of a superposition of trapping noise components
- From  $S$  vs.  $V_D$  data, the lateral position of defects can be determined
- From  $S$  vs.  $V_G$  data the vertical position in the gate-stack region can be determined
- From  $S$  vs.  $T$  data, the defect activation energy can be extracted



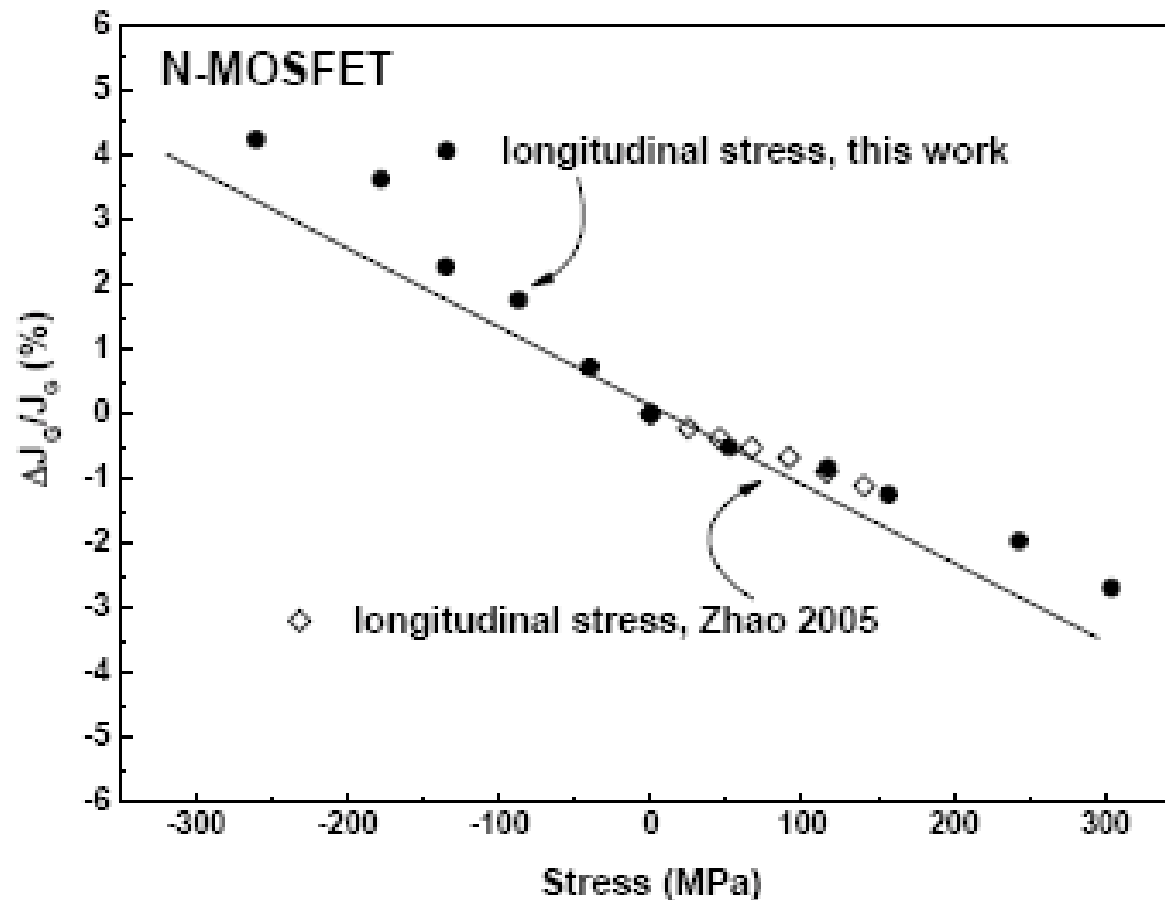
# Related Results and Preliminary Models

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- Related results
  - Stress dependence
    - Si MOSFET gate leakage currents
    - HfSiO, HfSiON dielectric constant
    - Time-dependent dielectric breakdown (TDDB)
- Forward/Inverse piezoelectric effect

# Strain Altered Gate Leakage of Si n-MOSFET

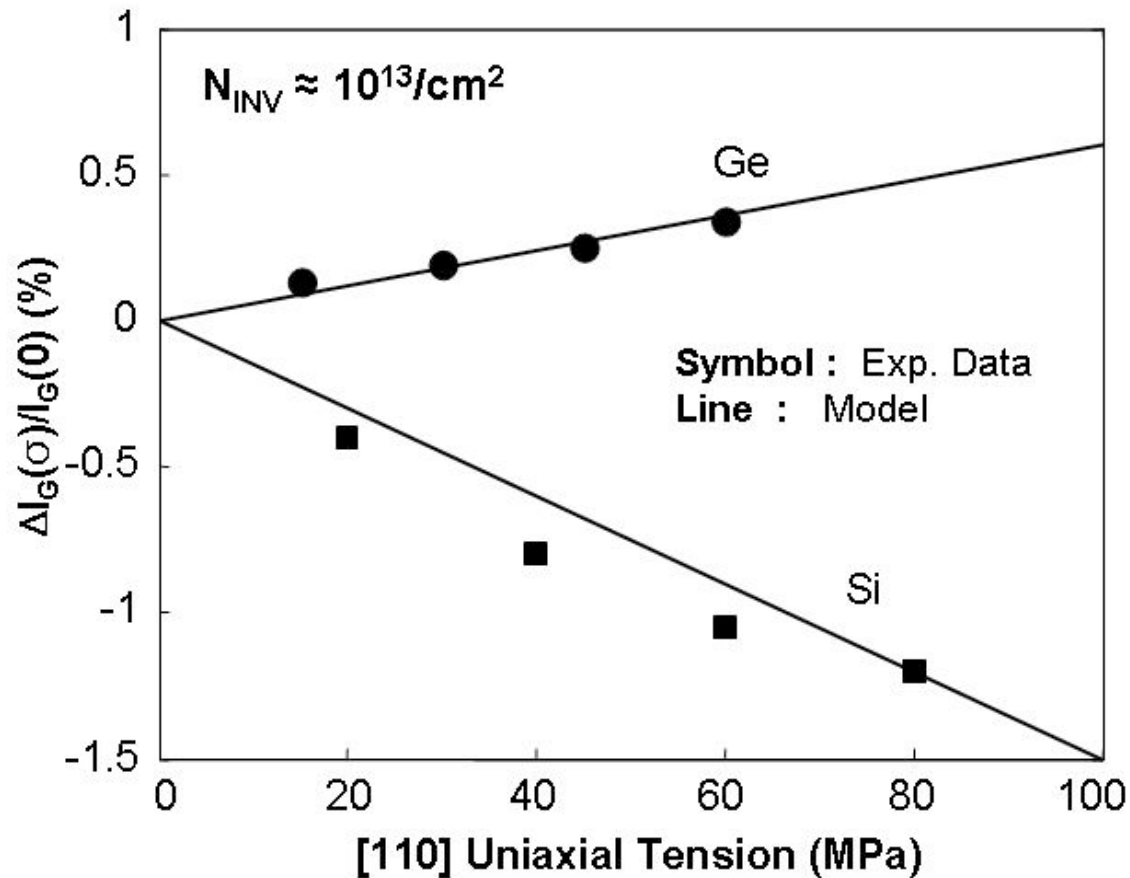
- Gate leakage increases/decreases with uniaxial longitudinal compression/tension along [110] direction



X. Yang et al. 2007  
Electron Device and and  
Semiconductor  
Technology

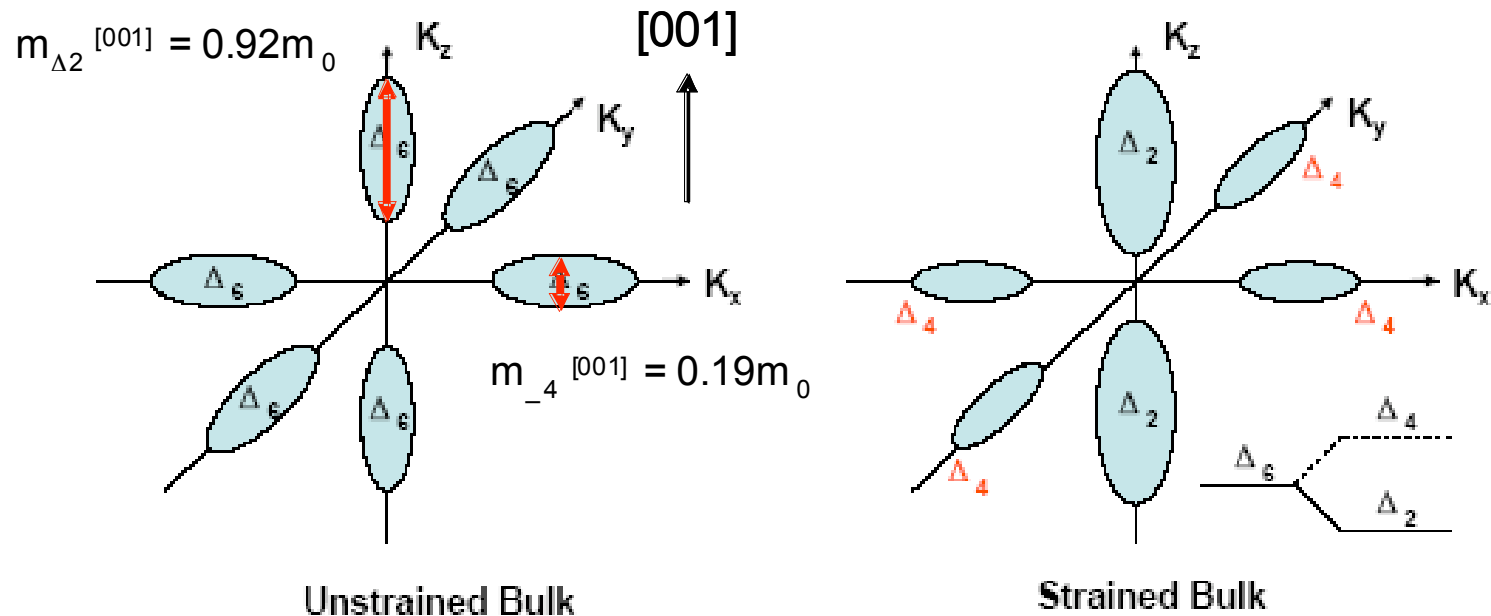
# Strain-Altered Gate Leakage of Ge & Si n-MOSFETs

- $I_G$  (Ge) increases, while  $I_G$  (Si) decreases with [110] uniaxial tension



Y.S. Choi et al. JAP 2007

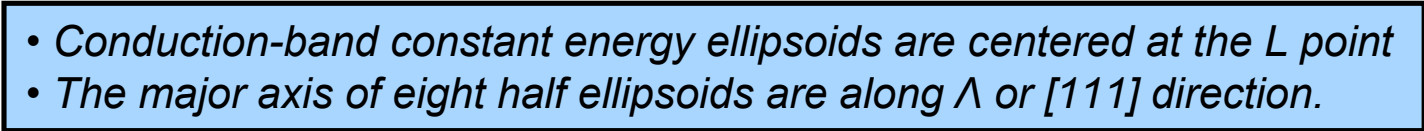
# Conduction Band Edge of Si



X. Yang et al. 2007  
Electron Device and and  
Semiconductor  
Technology

- Conduction-band constant energy ellipsoids are centered along the  $\Delta$  axis
- The major axis of six ellipsoids are along  $[100]$  direction.

*[110] Uniaxial Stress removes degeneracy and cause subband splitting*

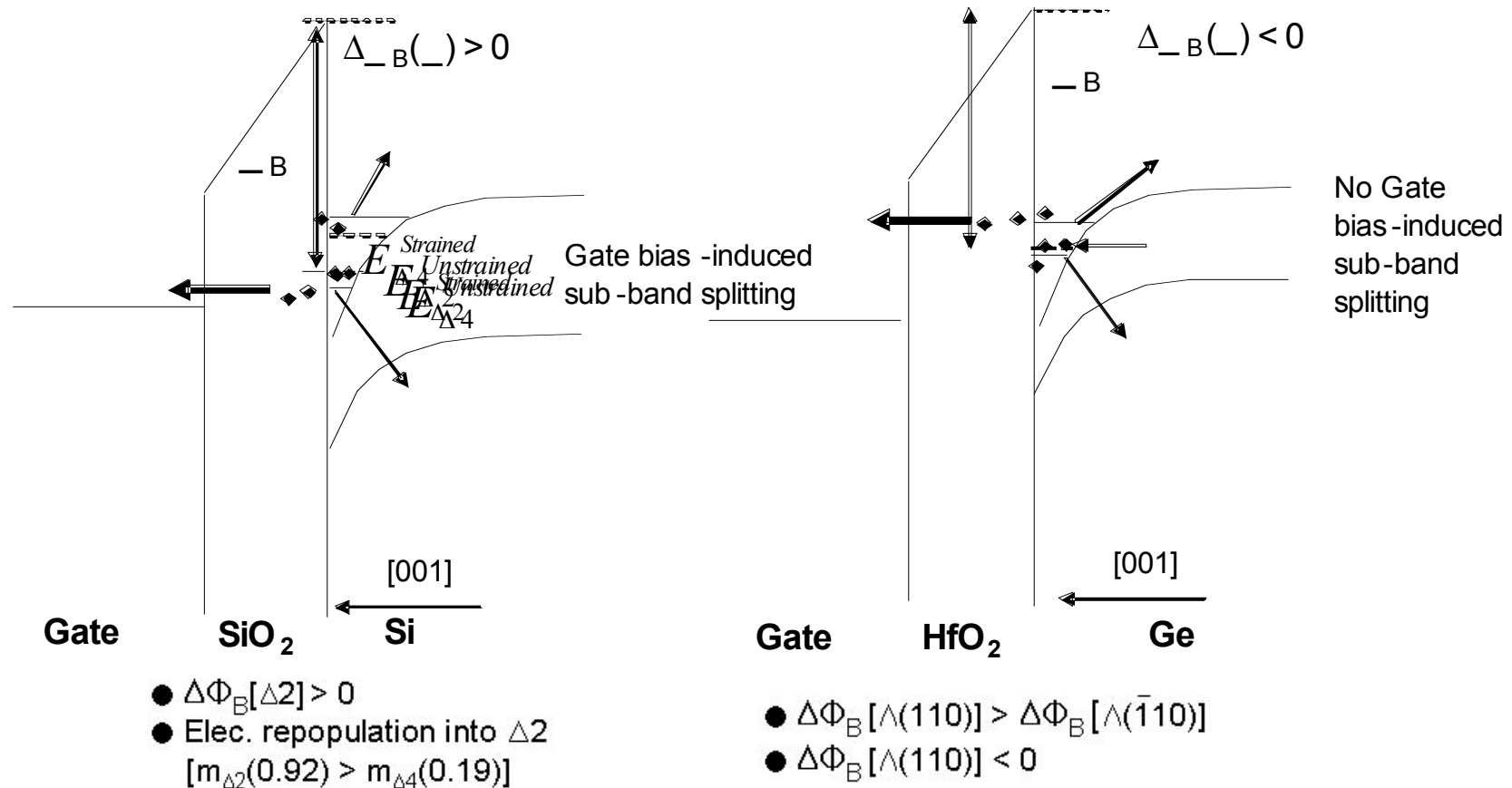


Only one out-of-plane effective mass ( $0.12m_0$ )

**Y.S. Choi et al. JAP 2007**

# Band Diagrams of Stressed Si & Ge n-MOSFETs

Tensile stress along [110] direction

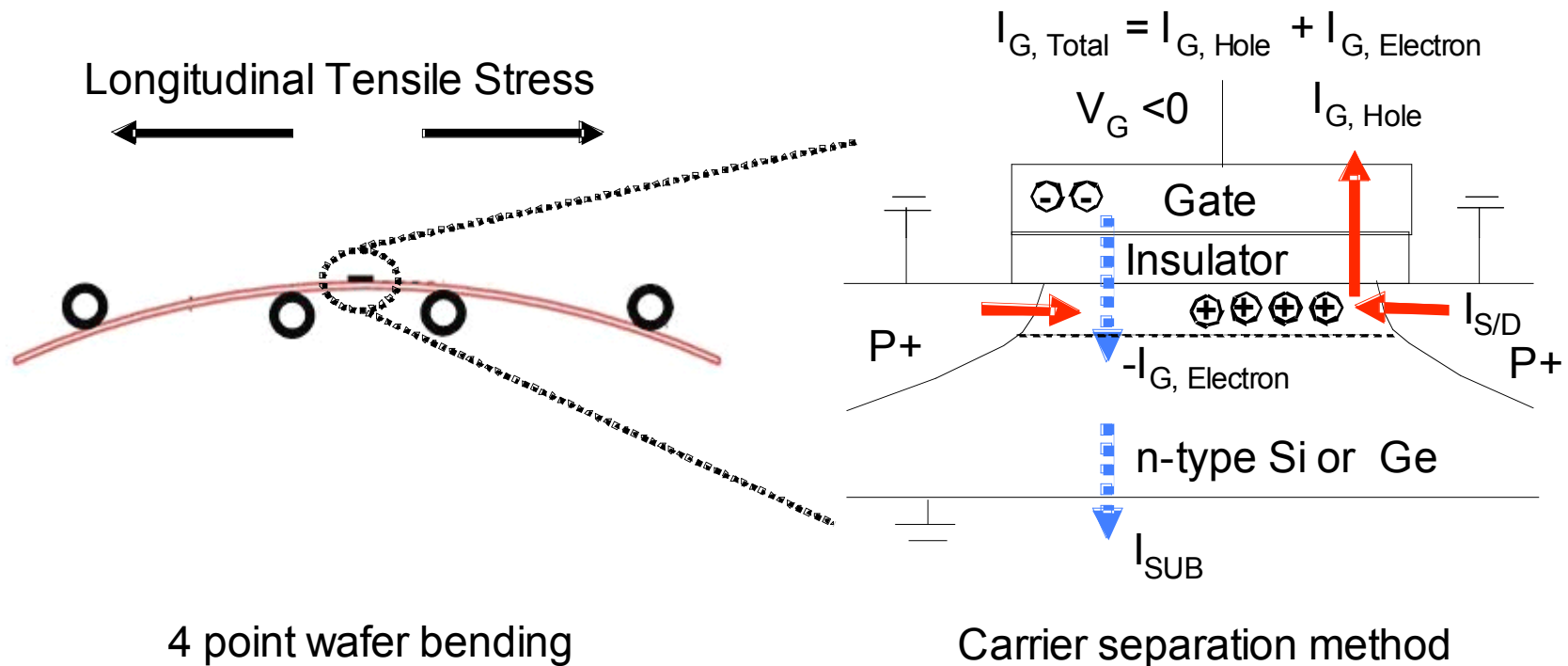


*$m^*$  increases due to repopulation  
 $\Rightarrow I_G$  decreases*

*$\Phi_B$  lowers due to band shift & splitting  
 $\Rightarrow I_G$  increases*



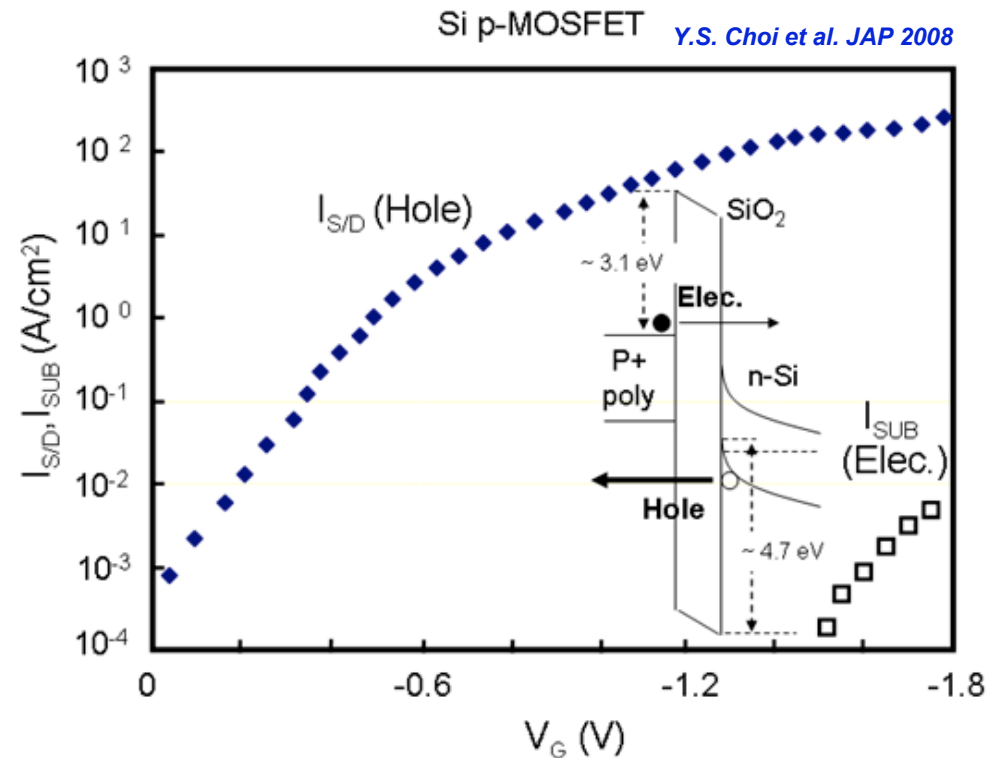
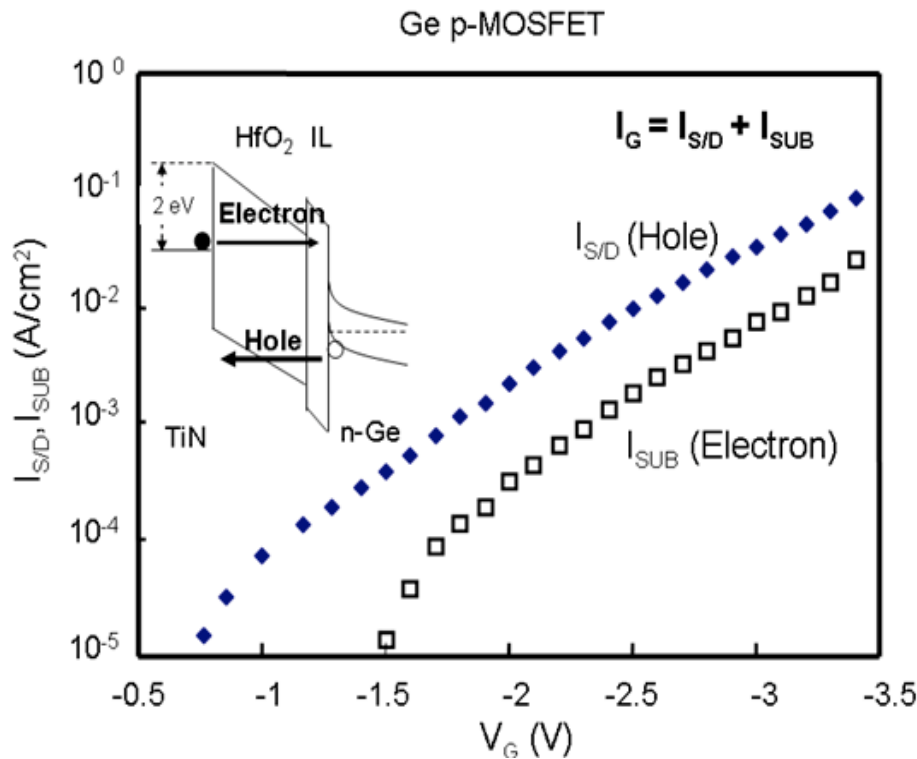
# 4-point wafer bending + Carrier Separation



Y.S. Choi et al. JAP 2008

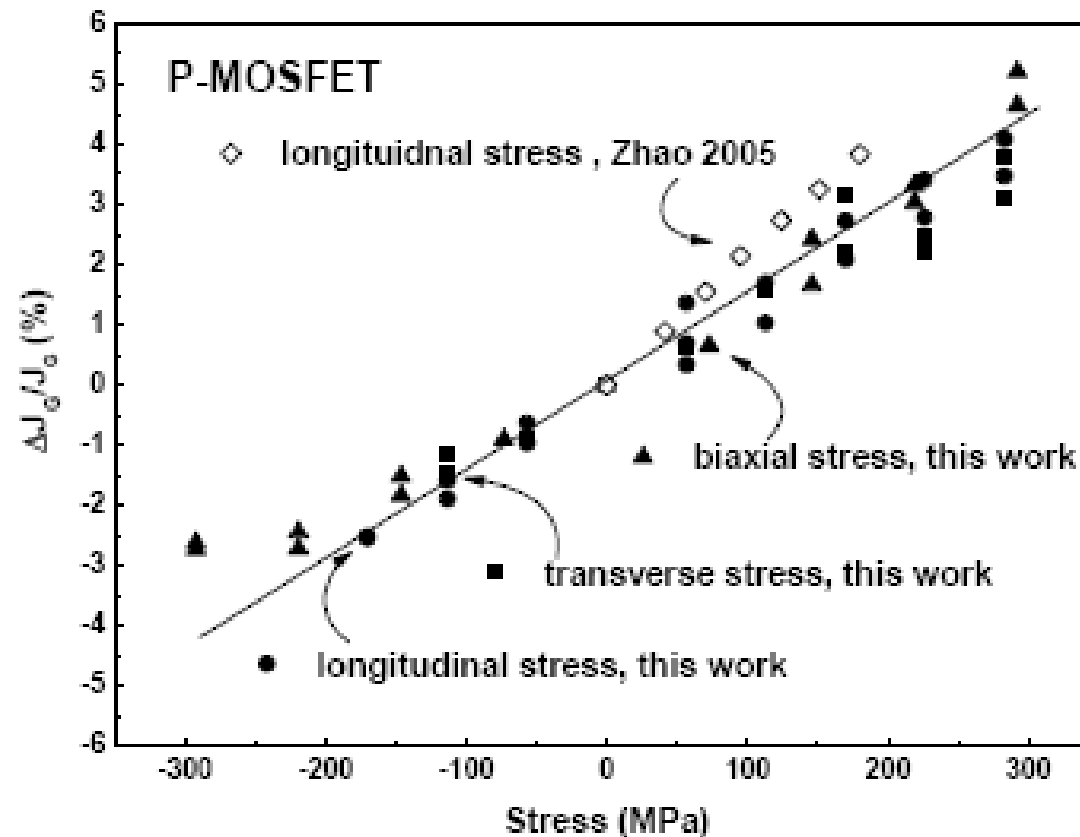
*Strain effect on each gate tunneling carrier (electron & hole) can be monitored!!*

# Carrier Separation of Si & Ge p-MOSFETs



- Hole tunneling from sub. is dominant for both Si & Ge p-MOSFETs
- $I_{SUB}/I_G(\text{Ge}) > I_{SUB}/I_G(\text{Si})$  due to metal gate in Ge device

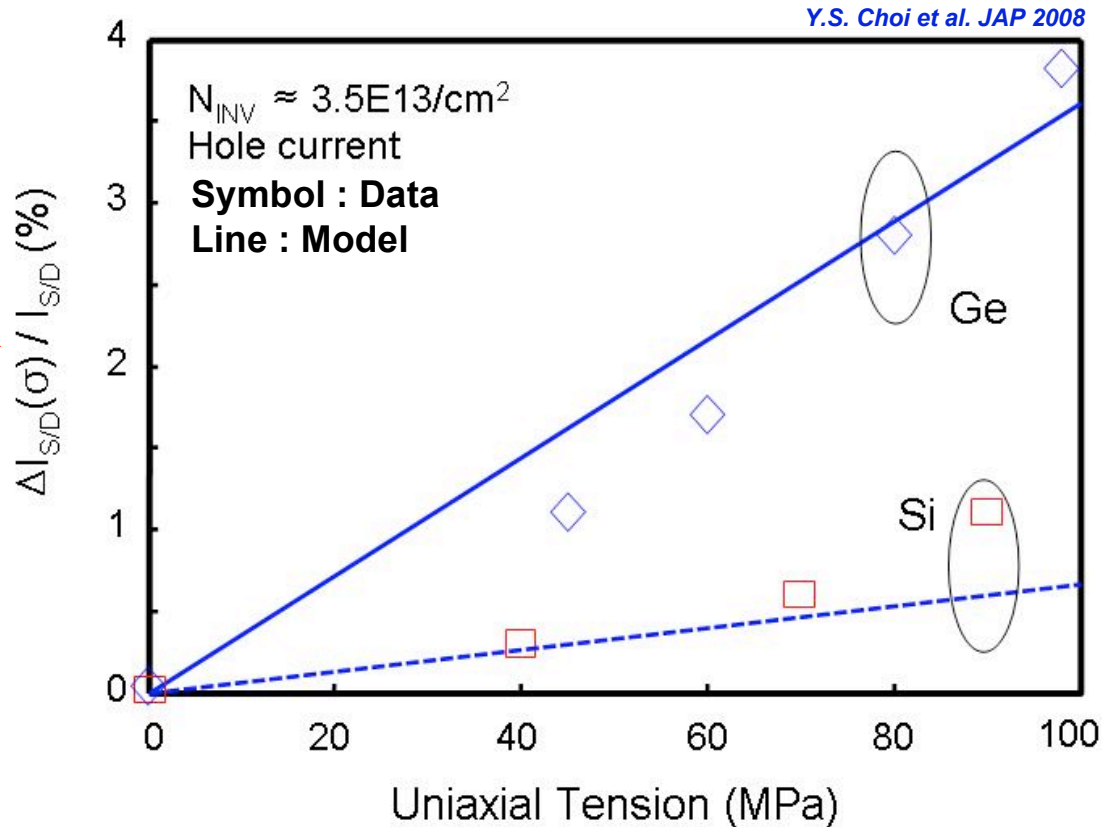
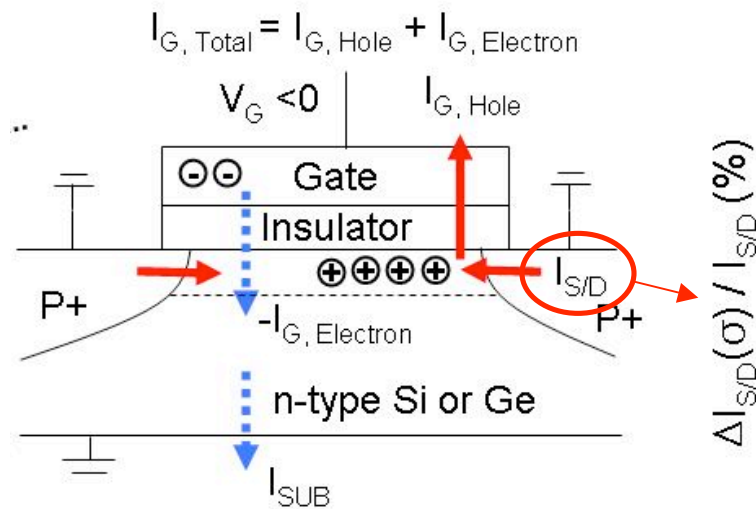
# Strain Altered Gate Leakage of Si p-MOSFET



X. Yang et al. 2007  
Electron Device and and  
Semiconductor  
Technology

$J_G$  decreases/increases with uniaxial longitudinal compression/tension along [110] direction

# Strain-Altered Gate Leakage Ge & Si p-MOSFETs from Inversion Layer

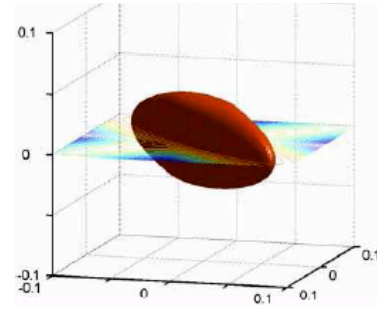
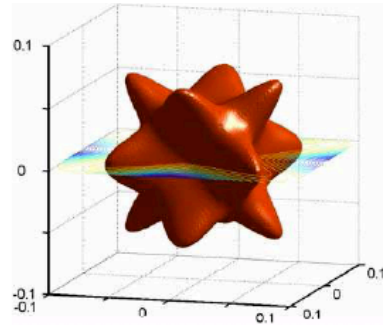


$$\Delta I_{S/D} / I_{S/D}^{Ge}(\sigma) > \Delta I_{S/D} / I_{S/D}^{Si}(\sigma)$$

# Same Physics for Holes in Si and Ge

Si

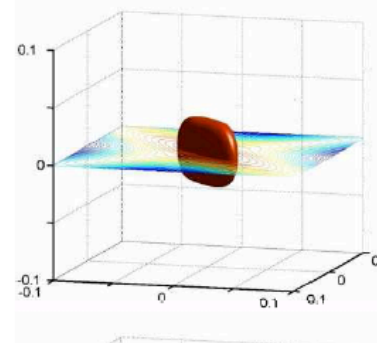
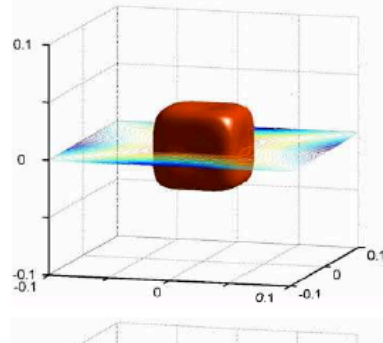
Si



Guangyu Sun  
Ph. D Dissertation 2007

Ge

Ge



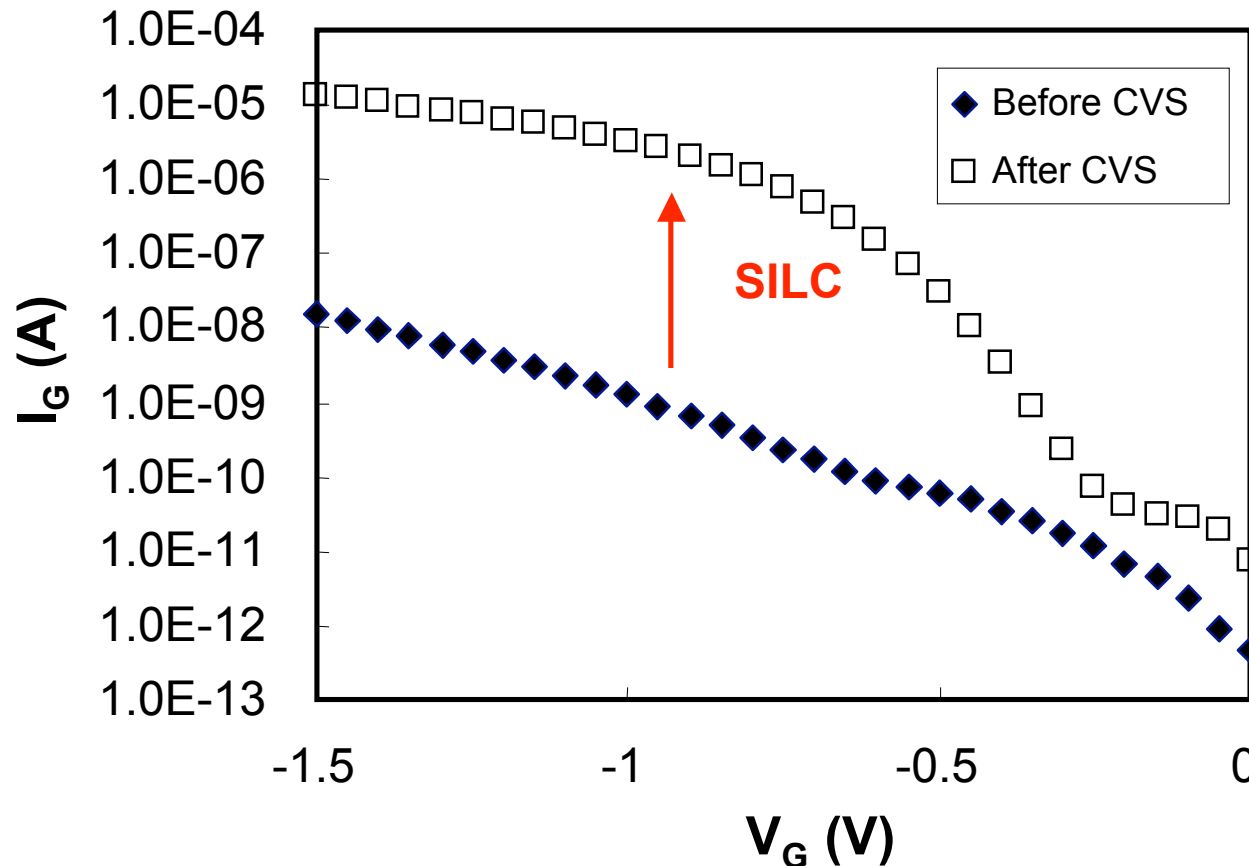
Unstressed

1GPa Uniaxial compression

- Same valence band edge for Si & Ge ( $\Gamma$ -point)
- Under applied stress, valence band edge shifts & splits with same manner, but based on different deformation potential constants of Si & Ge
- Different strain-altered effective mass & subband splitting

# Constant Voltage Stressing (CVS)

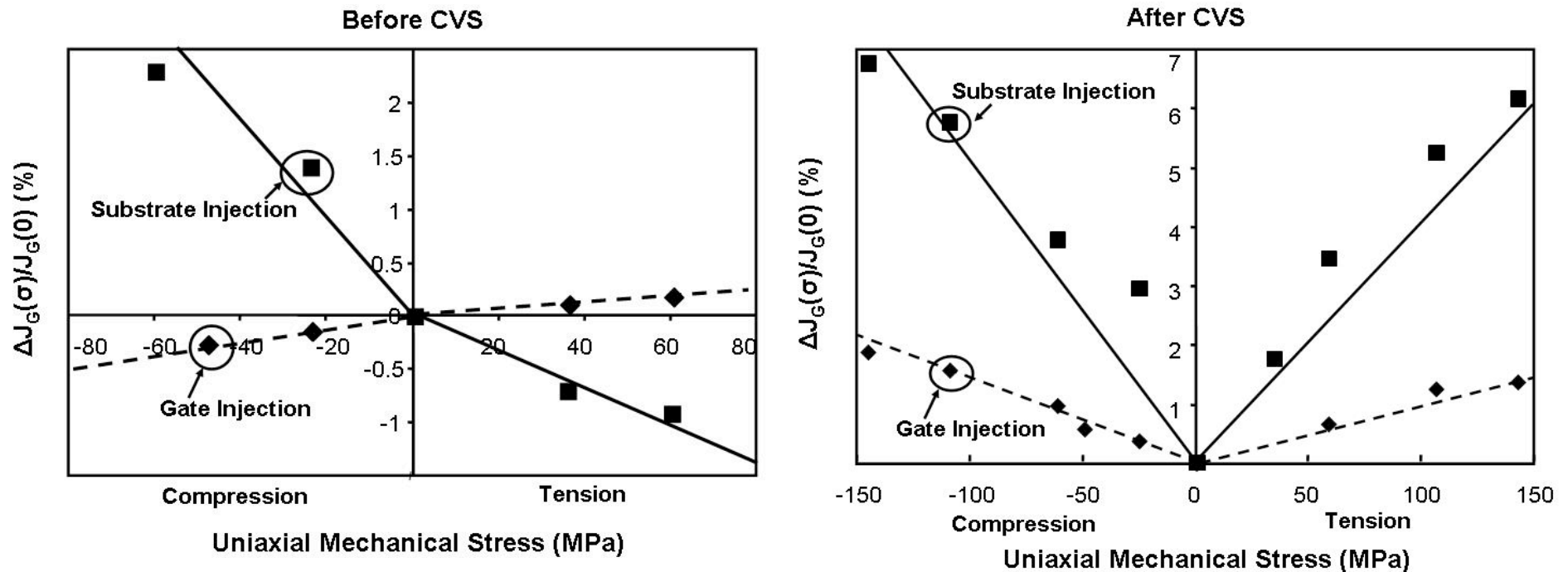
**SILC = Stress Induced Leakage Current**



- Stressing Condition  
= -4 V for 50 Sec
- Sample Structure  
= TaN/2.5 nm SiO<sub>2</sub>/p-Si
- Area of Sample  
=  $10^5 \mu\text{m}^2$

*High-field stress (Fowler-Nordheim stress) generates electron traps in the SiO<sub>2</sub>/Si interface that facilitate trap-assisted tunneling*

# Strain Altered Gate Leakage Before and After CVS

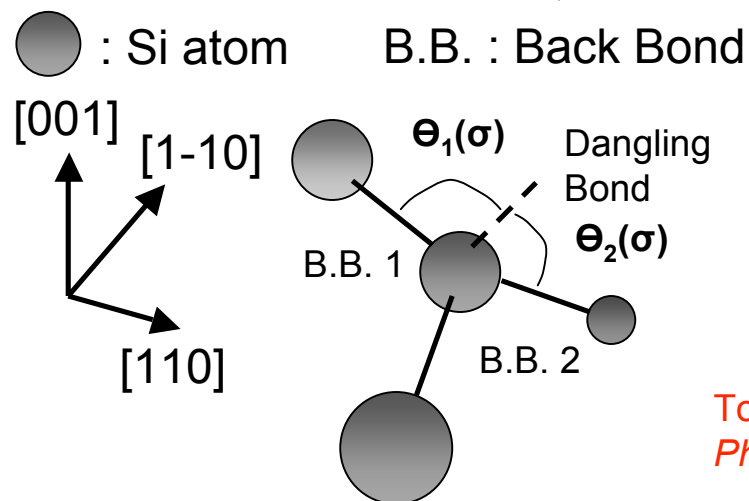
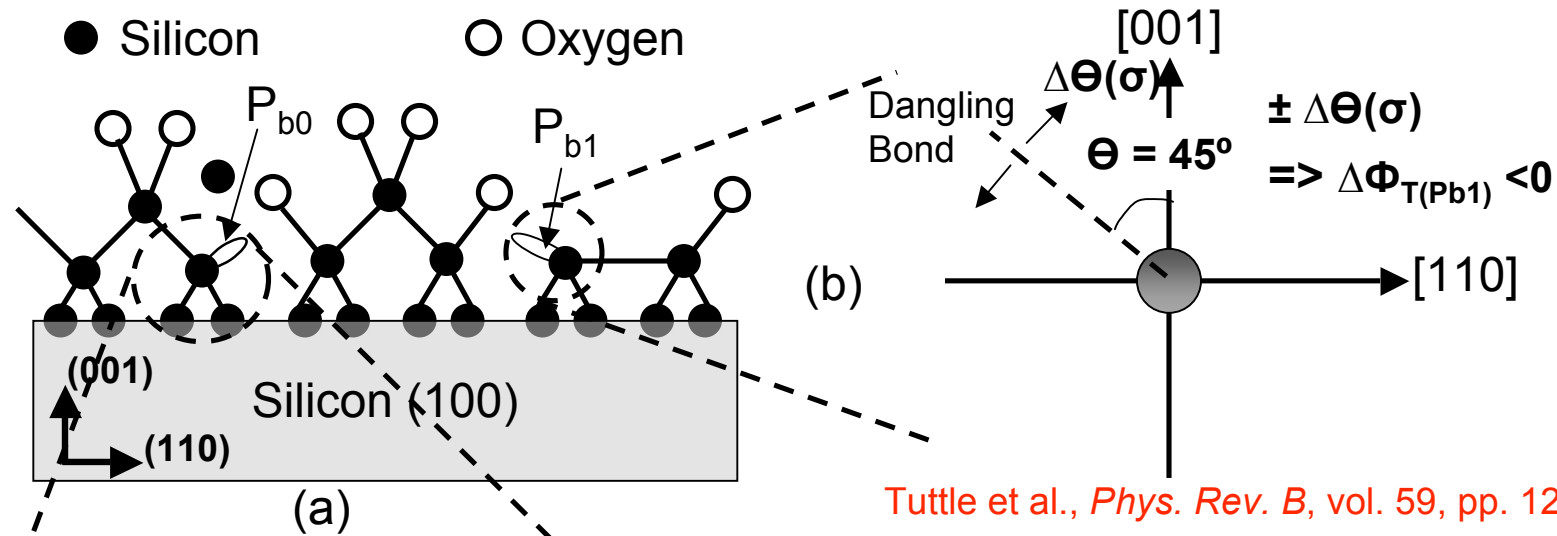


*Before CVS=> An opposing uniaxial stress dependence between Gate and Sub. Injections*

*After CVS=> Both gate and sub. Injections increase with uniaxial [110] stress*



# [110] Uniaxial Stress vs Interface Trap $E_A$



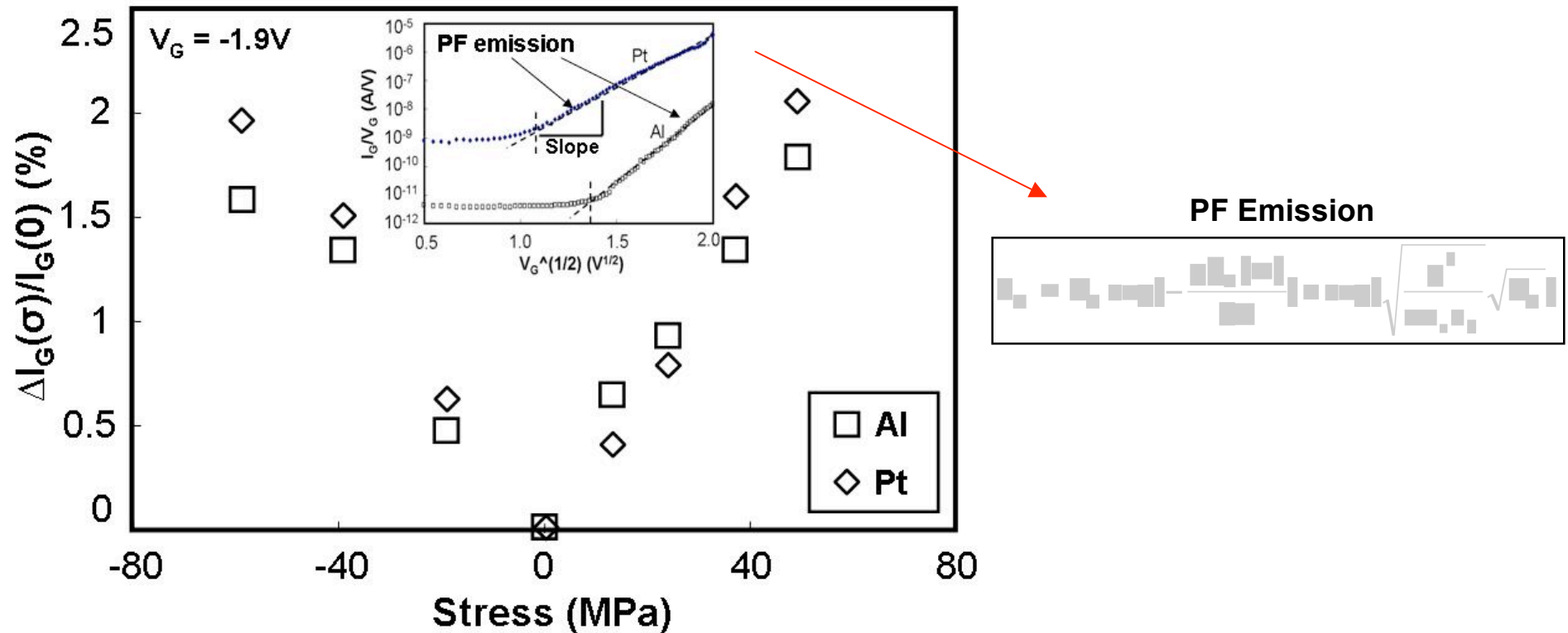
|         | $\theta_1(\sigma)$   | $\theta_2(\sigma)$   | $\Phi_{T(Pb0)}(\sigma)$ |
|---------|----------------------|----------------------|-------------------------|
| Comp.   | $\Delta\theta_1 < 0$ | $\Delta\theta_2 > 0$ | $\Delta\Phi_T < 0$      |
| Tension | $\Delta\theta_1 > 0$ | $\Delta\theta_2 < 0$ | $\Delta\Phi_T < 0$      |

Toda et al., *IEEE International Reliability Physics Symposium*, San Jose, 2005.

[110] tensile & compressive stresses decreases trap activation energy

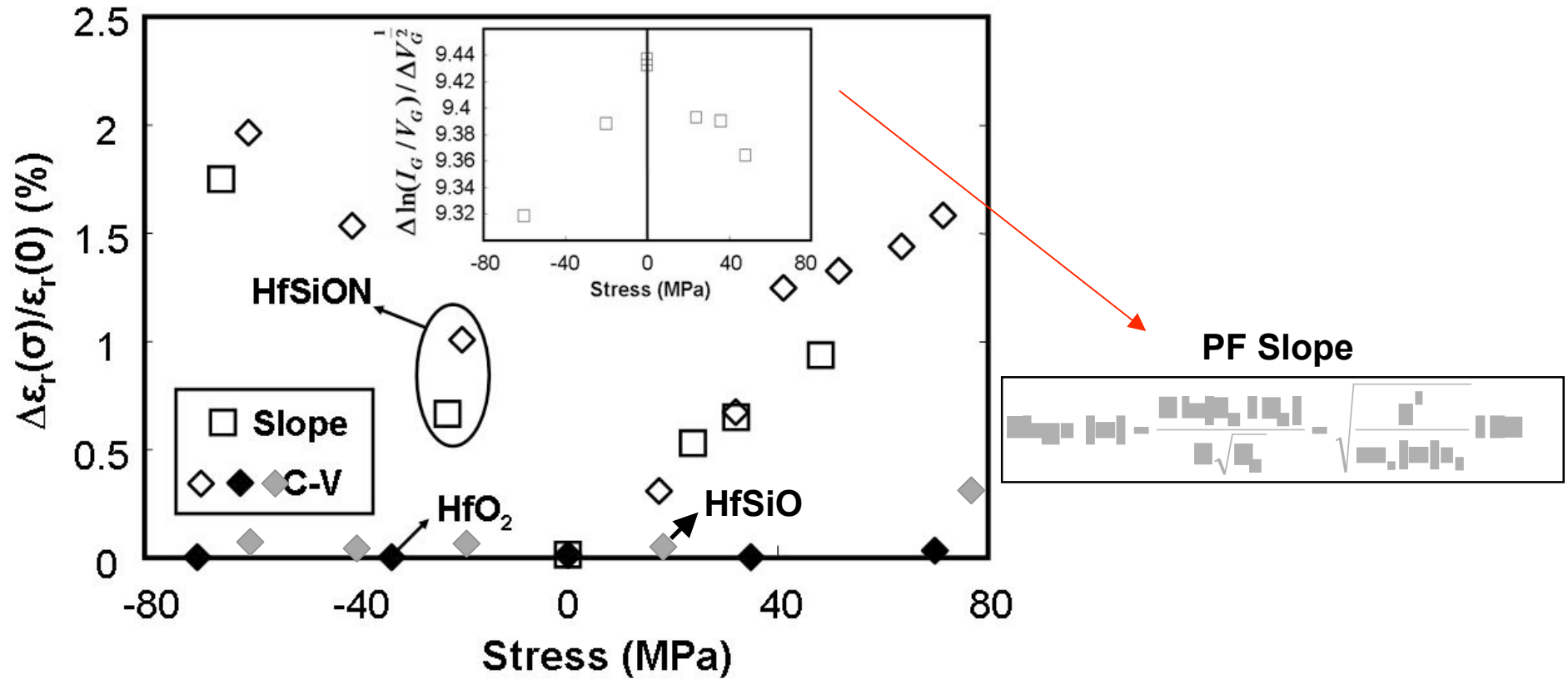


# Stress Effect on Gate Leakage in HfSiON



- *PF Emission => Trap-Assisted Gate Tunneling*
- *$I_G$  increases with both [110] uniaxial tension & compression*

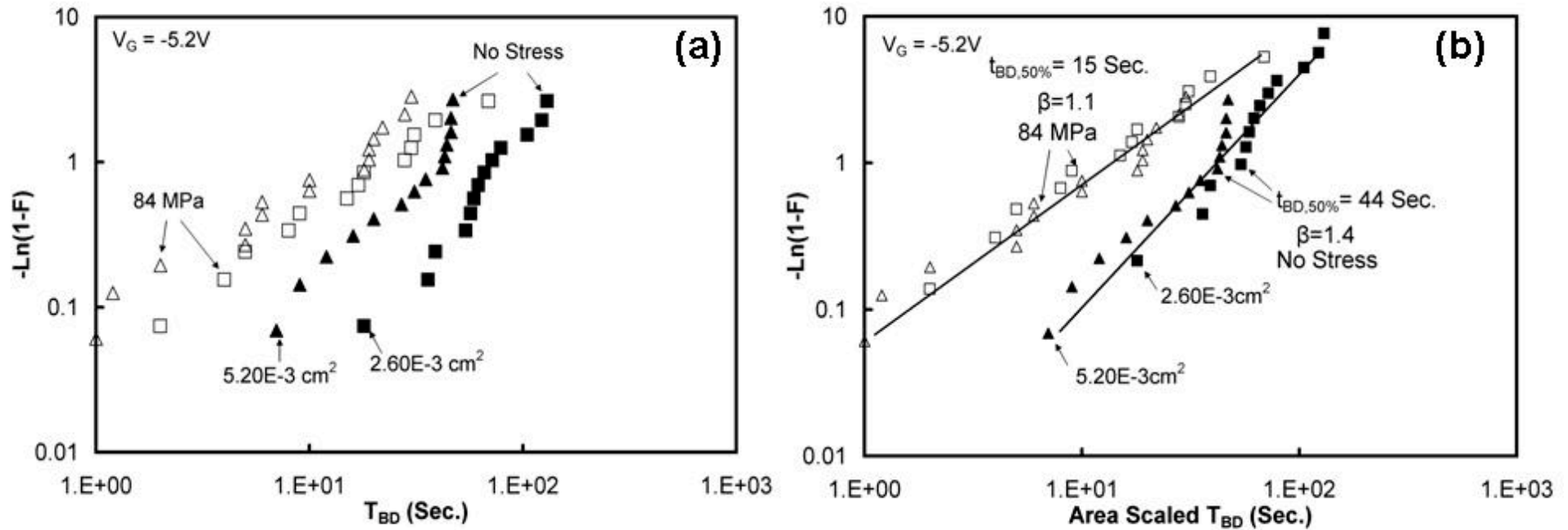
# Stress Effect on Dielectric Constant of HfSiON



- $\epsilon_r$  of HfSiON increases with both tension and compression
- Nitrogen incorporation ~ Strain effect on  $\epsilon_r$

# Stress Effect on TDDB

## Uniaxial Tension



- TDDB on Al-gate HfSiON on p-Si MOS capacitor decreases with tensile stress

# Related Results and Preliminary Models

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- Related results
  - Stress dependence
    - Si MOSFET gate leakage currents
    - HfSiO, HfSiON dielectric constant
    - Time-dependent dielectric breakdown (TDDB)
- Forward/Inverse piezoelectric effect

# Piezoelectric Effect

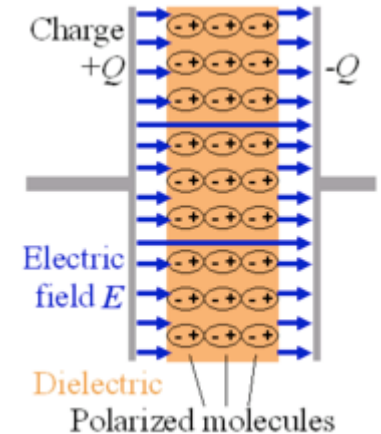
**Piezoelectricity: Effect of nonvanishing electric field (polarization) induced by strain.**

The fundamental cause of piezoelectricity: *lack of a center of inversion*.  
No piezoelectric effect in elementary semiconductors.

Example of semiconductors having piezoelectricity

**GaAs:** zinc-blende

**GaN:** wurtzite



**GaAs:** Only  $e_{44} \neq 0$

$$\begin{pmatrix} P_x \\ P_y \\ P_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & e_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & e_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & e_{44} \end{pmatrix} \begin{pmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{yz} \\ \epsilon_{zx} \\ \epsilon_{xy} \end{pmatrix}$$

Polarization
Piezoelectric tensor
Strain

**GaN:**  $e_{13} \neq 0$ ,  $e_{33} \neq 0$ , and  $e_{15} \neq 0$

$$\begin{pmatrix} P_x \\ P_y \\ P_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{yz} \\ \epsilon_{zx} \\ \epsilon_{xy} \end{pmatrix}$$

**Inverse Piezoelectric Effect: Strain induced by applied electric field.**

# Modeling Cumulative Effect of Stress on Reliability

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- Open questions
  - Relative contribution of fixed/variable mechanical stressors
    - Fabrication
    - Bias/ inverse piezoelectric effect
    - Package/encapsulation/thermal mismatch
  - Bond configuration change
  - Model as electrical-mechanical-temperature-optical stress dependent generation cross-section?
  - Incorporation into FLOOPS reliability simulations
  - Characterization/modeling/simulation feedback loop
  - ???